ERROR RATE AND POWER DISSIPATION IN NANO-LOGIC DEVICES

A Thesis

by

JONG UN KIM

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2004

Major Subject: Electrical Engineering

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Approved as to style and content by:

Laszlo B. Kish (Chair of Committee)	
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ABSTRACT

Error Rate and Power Dissipation in Nano-Logic Devices.
(May 2004)
Jong Un Kim, B.S.; M.S.; Ph.D., Seoul National University
Chair of Advisory Committee: Dr. Laszlo B. Kish

Current-controlled logic and single electron logic processors have been investigated with respect to thermal-induced bit error. A maximal error rate for both logic processors is regarded as one bit-error/year/chip. A maximal clock frequency and an information channel capacity at a given operation current are derived when a current-controlled logic processor works without error. An available operation range in a current-controlled processor with 10^8 elements is discussed. The dependence of an error-free condition on temperature in single electron logic processors is derived. The size of the quantum dot of a single electron transistor is predicted when a single electron logic processor with the 10^9 single electron transistors works without error at room temperature.

To My Wife, Rira

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1. INTRODUCTION

The technology of semiconductor processing has been developed according to Moore's law. Simply speaking, Moore's law suggests that the size of an integrated circuit with MOSFET decreases exponentially every year. The 2003 International Technology Roadmap for Semiconductors (ITRS) showed that the scaling factor was 0.7 per year. It also predicted that the DRAM half-pitch, so called characteristic length, will be 45 nm in 2010. Since the size of a unit MOSFETs decreases, the microprocessor will get faster. However, Kish reported that Johnson-Nyquist thermal noise would be a serious problem when semiconductor industries keep reducing the size of transistor and increasing the clock frequency at the same time [1]. The thermal noise is also applicable to any processor including nano-scalar processor.

A digital processor works in voltage-controlled, current-controlled or single electron logic. Logic states in voltage-controlled and current-controlled logic depend on voltage and current, respectively. Logic states in single electron logic are dependent on a single electron. That is to say, a single electron represents 'on' state in single electron logic. The MOSFET microprocessor works in the voltage-controlled logic, but until now no processor has been operated in current-controlled logic or single electron logic. However, a processor with single electron transistor can work in current-controlled logic or single electron logic.

Single electron transistor has two single electron junctions and one Coulomb island (or quantum dot). Single electron junction is ultrasmall junction at which single electron tunneling is observed. The single electron tunneling has been observed in granular metallic structure since the 1950s. A granular metallic structure is thought of as a structure consisting of source, ultrasmall grain called Coulomb island, and drain, like single electron transistor. They are separated by insulator. The single electron tunneling phenomena occurs only when the island is small enough for its potential variation to affect a successive tunneling event at each junction. Otherwise, the tunneling of electron at each junction is uncorrelated Poisson process like tunneling at a single energy barrier. Fulton and Dolan reported that current in the single electron transistor with the nanoscale island can be

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This thesis follows the style of *Fluctuation and Noise Letters*.

controlled by gate voltage [2]. Likharev and Semenov introduced single electron logic in 1987 [3]. Most of single electron logic processors consist of single electron transistors [3, 4, 5]. So far every single electron device is available only at temperature lower than 4 K. Single electron transistor cannot be an elementary component in the voltage-controlled logic processor, since a voltage gain is too small for the logic processor [6].

In this thesis, we consider current-controlled logic and single electron transistor in single electron logic. The current-controlled logic and the single electron logic are taken into consideration in section 2 and section 3, respectively.

2. CURRENT-CONTROLLED LOGIC PROCESSORS*

As we mentioned it, Kish predicted that Johnson-Nyquist thermal noise would be a serious problem in a modern MOSFET microprocessor in near future. Considering the effective noise voltage and the power dissipation of the MOSFET processor, he showed that the clock frequency and the number of the transistors in a chip could not increase together at about 30 nm characteristic length of the microprocessor.

In this chapter, we consider a processor with current-controlled logic. Suppose that shot noise is the dominant noise source in the processor. We assume that noise margin is 60 % of a on-state current as it is 60 % of an on-state voltage in a MOSFET processor with voltage-controlled logic.

If the shot noise is a full shot noise, the one-sided power density spectrum of the shot noise is $2Ie$, where I is the on-state current and e the electron charge. For a single gate, Rice's generalized formula [1] gives error rate

$$\nu_f(I, f_c) = \frac{2}{\sqrt{3}} f_c \exp\left(-\frac{9}{100}\frac{I}{f_c e}\right) \tag{2.1}$$

where f_c is the cutoff frequency, which is roughly equal to the highest possible clock frequency, of the processor. Figure 2.1 shows the error rate as a function of the cutoff frequency at a given on-state current. As shown in Figure 2.1, the error rate in the processor increases very rapidly with increasing the cutoff frequency.

A reasonable assumption for the upper limit of acceptable noise-induced bit error rate, i.e., maximal error rate, is one bit-error/chip/year, i.e., $f_{year} = 3.17 \times 10^{-8}$ Hz. Combining Eq. (2.1) and f_{year}, the maximum cutoff frequency, i.e., maximal clock frequency, $f_{c,max}$, in the processor with N transistors is given by[1]:

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[1] Equation (2.1) at $\nu_f = f_{year}/N$ is also solved by numerical method. The maximum cutoff frequency obtained by bisection method is the same as by Eq. (2.2). The values of the Lambert W-function are evaluated in Matlab. Figures 2-2 and 2-3 are plotted on the basis of Eq. (2.2).

$$f_{c,max} = \frac{\sqrt{3}}{2}\frac{f_{year}}{N}\exp\left[w\left(\frac{3\sqrt{3}}{50}\frac{I}{e}\frac{N}{f_{year}} \right) \right] \tag{2.2}$$

where $w(x)$ is the Lambert W-function [7]. Since the Lambert function, $w(x)$, can be approximated by $\ln x - \ln(\ln x)$ for $x >> 3$, the maximal clock frequency is approximated as follows:

$$f_{c,max} \approx \frac{9}{100}\frac{I}{e}\left[\ln\left(\frac{3\sqrt{3}}{50}\frac{I}{e}\frac{N}{f_{year}} \right) \right]^{-1} \quad . \tag{2.3}$$

Figure 2.2 shows $f_{c,max}$ as a function of the on-state current. The dotted lines represent Eq. (2.3), and the solid ones represent Eq. (2.2) in Figure 2.2. As shown in Figure 2.2, the approximation seems to be a good estimation of the maximal clock frequency of the processor with the maximal error rate. In Figure 2.2, the thin solid line represents the maximal clock frequency of a single element processor and the thick solid line represents that of a 10^8 element processor. It is apparent that the maximal clock frequency is almost independent of the number of the elements in the processor.

The information channel capacity, C_i, of a single channel is given by Shannon information formula:

$$C_i = B\ln\left(1 + P_{signal}/P_{noise}\right) \tag{2.4}$$

where B is the clock frequency of signal which can be approximated by the clock frequency in the logic processor, and P_{signal} and P_{noise} are power of signal and noise, respectively. Since the signal is a square wave, P_{signal}/P_{noise} can be approximated as the ratio of the clock frequency to the error rate. Provided all of the transistor processes are independent, the upper limit of information channel capacity can be written as:

$$C_i = N\, f_{c,max} \ln\left(1 + \frac{f_{c,max} N}{f_{year}} \right) \quad . \tag{2.5}$$

Figure 2.3 shows the information channel capacity at the maximal clock frequency. As shown in Figures 2.2 and 2.3, the maximum clock frequency and the information channel capacity increase monotonically with increasing the on-state current. The shaded area in

two figures is the available operation range of a 10^8 element processor if the maximal supply current is 100 Ampere.

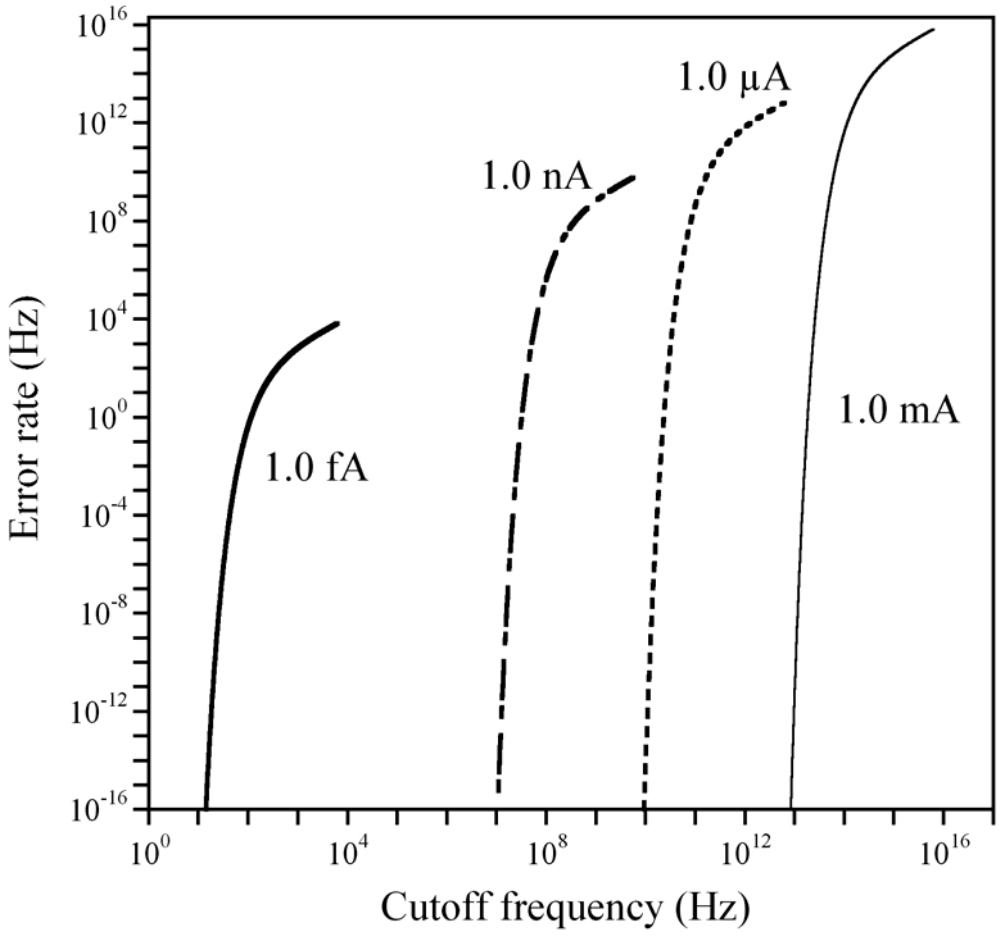

Figure 2.1. Error rate of a single transistor in a current-controlled logic processor. Each number represents the on-state current.

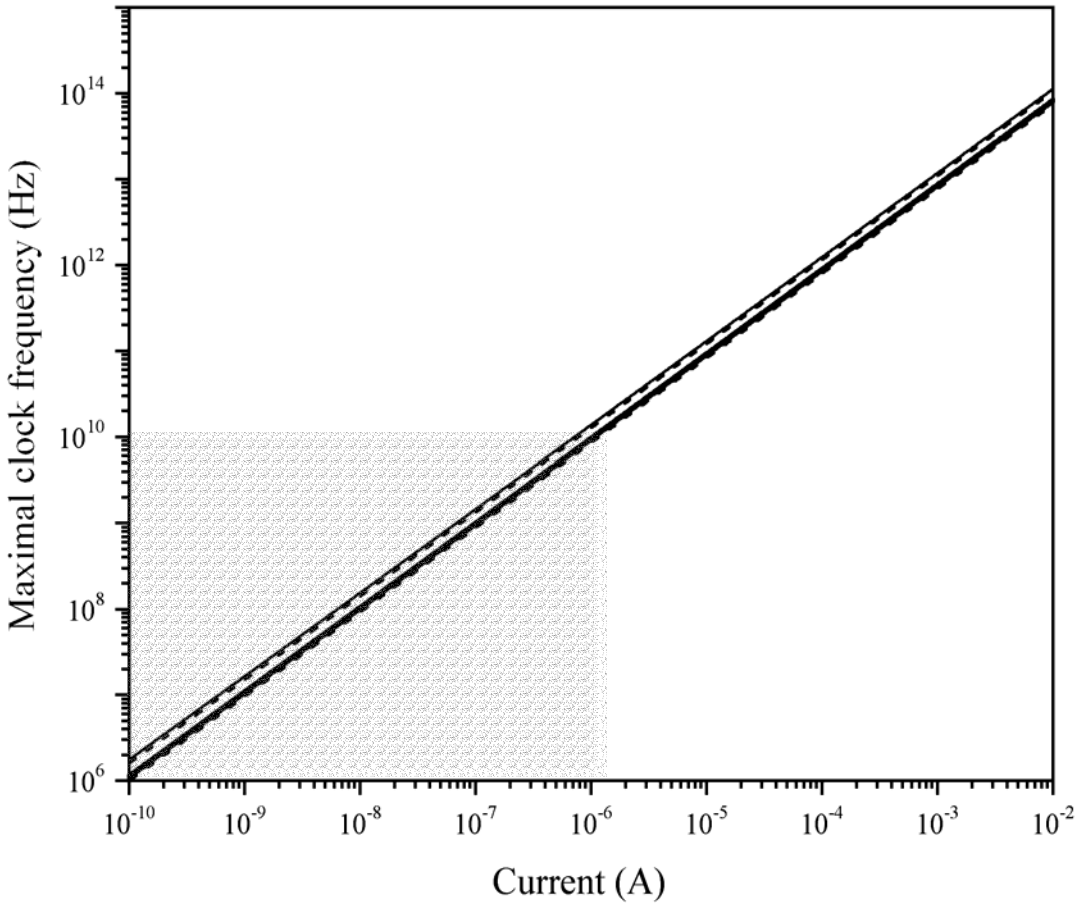

Figure 2.2. Maximal clock frequency of the processor that works within the maximal error rate. The solid lines are from Eq. (2.2) and the dotted lines are from Eq (2.3). The thin line (upper line) represents the case of a single transistor and the thick one (lower line) represents a 10^8 transistor processor. The shaded area is the possible operation range in a 10^8 transistor processor with 100 A upper limit of the supply current.

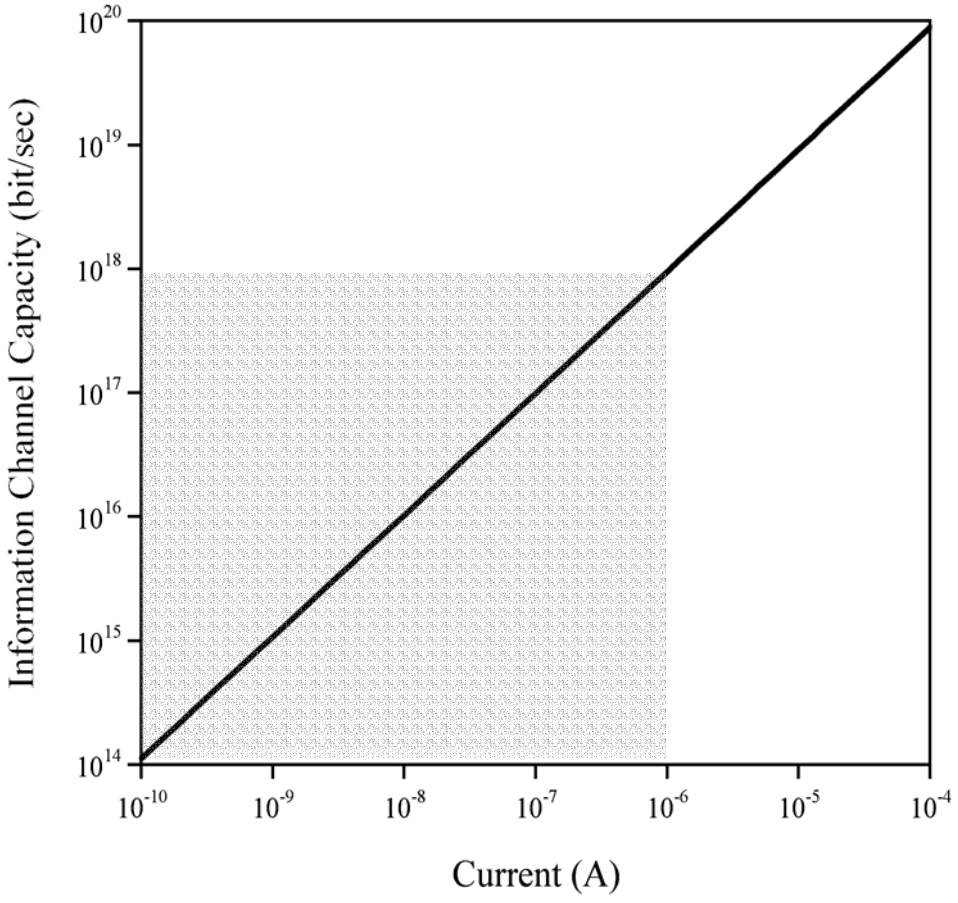

Figure 2.3. Upper limit of information channel capacity at the maximum clock frequency. The thin solid line represents the one transistor and the thick the processor including 10^8 transistors. The shaded area is the possible operation range in a 10^8 transistor processor with 100 A upper limit of the supply current.

3. SINGLE ELECTRON LOGIC PROCESSORS*

During the last decade single electron tunneling at ultra-small junction has received a great deal of attention in nanoelectronics. Two pre-requirements for the satisfactory on/off switching operation of a single ultrasmall junction are related to the capacitance, C, and the tunneling resistance, R_T, of the single junction[8, 9]. Firstly, the tunneling resistance of the ultrasmall junction has to be much greater than the resistance quantum $R_K = h/e^2 \cong$ 25.8 kΩ. This condition is required since the energy uncertainty associated with the tunneling lifetime, $\tau_T = R_T C$, should be much smaller than the electrostatic charging energy $E_C = e^2/2C$. Secondly, the electrostatic charging energy should be much greater than the thermal fluctuation energy, which requirement results in

$$C < e^2/k_B T \quad , \tag{3.1}$$

where k_B is the Boltzmann constant and T is the temperature. The first condition leads to the required discrete energy levels for single electron tunneling, and the second one to the blockade of the thermally assisted tunneling. The single electron tunneling has been observed at very low temperatures (< 4 K) [10], where both requirements are easily satisfied by today's technology. A variety of single electron tunneling devices – transistors [2], electrometers [11], sensors [12], switch [13], etc.- have been reported to successfully operate at low temperatures.

In single electron logic processors, logic levels are dependent on a single electron. Likharev and Semenov [3], Averin and Likharev [4], and Korotkov [6] proposed single electron logic gates and circuitry. They used the single electron transistor as the basic component of these circuits. However, at non-zero temperature, thermally assisted tunneling takes place even at such biased control voltages where the device would have closed at zero temperature [4]. Apparently, this phenomenon leads to bit flip errors. Error-free performance is thought of as that a logic processor works within the maximal error

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rate, i.e., one bit-error/chip/year In single electron logic processors, this limit corresponds to one electron/chip/year.

3.1. Error-free Condition

We consider a single electron transistor, with double single electron junction, including a gate capacitor and a quantum dot, with low impedance driving and outputting, i.e., $Z_1, Z_2, Z_G \langle\langle R_K, \omega^{-1}C_1^{-1}, \omega^{-1}C_2^{-1}, \omega^{-1}C_G^{-1},$ as shown in Figure 3.1. The single electron tunneling rates at the single junction [14] and in single electron transistor [15] are reviewed in appendix. Under these low-impedance conditions, the single electron tunneling rate through each junction is expressed as follows (see Eqs. (A.11) and (A.12)):

$$\vec{\Gamma}_1 = \frac{1}{e^2 R_1}\frac{E_{1r}(V, V_G, ne)}{1-\exp\left[-\beta E_{1r}(V, V_G, ne)\right]} = \frac{k_B T}{e^2 R_1}\frac{\eta_{1r}}{1-\exp(-\eta_{1r})} \tag{3.2a}$$

$$\overleftarrow{\Gamma}_1 = \frac{1}{e^2 R_1}\frac{E_{1l}(V, V_G, ne)}{\exp\left[\beta E_{1l}(V, V_G, ne)\right]-1} = \frac{k_B T}{e^2 R_1}\frac{\eta_{1l}}{\exp(\eta_{1l})-1} \tag{3.2b}$$

$$\vec{\Gamma}_2 = \frac{1}{e^2 R_2}\frac{E_{2r}(V, V_G, ne)}{1-\exp\left[-\beta E_{2r}(V, V_G, ne)\right]} = \frac{k_B T}{e^2 R_2}\frac{\eta_{2r}}{1-\exp(-\eta_{2r})} \tag{3.2c}$$

$$\overleftarrow{\Gamma}_2 = \frac{1}{e^2 R_2}\frac{E_{2l}(V, V_G, ne)}{\exp\left[\beta E_{2l}(V, V_G, ne)\right]-1} = \frac{k_B T}{e^2 R_2}\frac{\eta_{2l}}{\exp(\eta_{2l})-1} \tag{3.2d}$$

where $\vec{\Gamma}$ and $\overleftarrow{\Gamma}$ are the single electron tunneling rates through the junction in a left-to-right and a right-to-left directions, respectively. The subscript number represents the different junctions, and the subscripts *r* and *l* represent the direction that an electron tunnels from left to right and from right to left, respectively. R is the tunneling resistance, $\beta = 1/k_B T$, and n is the number of the excess charge on the quantum dot. The tunneling-related energies in Eq. (3.2) are defined by

$$E_{1r}(V, V_G, ne) = \frac{e}{C_\Sigma}\left[\left(C_2 + \frac{C_G}{2}\right)V + C_G V_G + ne - \frac{e}{2}\right] \tag{3.3a}$$

$$E_{1l}(V, V_G, ne) = \frac{e}{C_\Sigma}\left[\left(C_2 + \frac{C_G}{2}\right)V + C_G V_G + ne + \frac{e}{2}\right] \tag{3.3b}$$

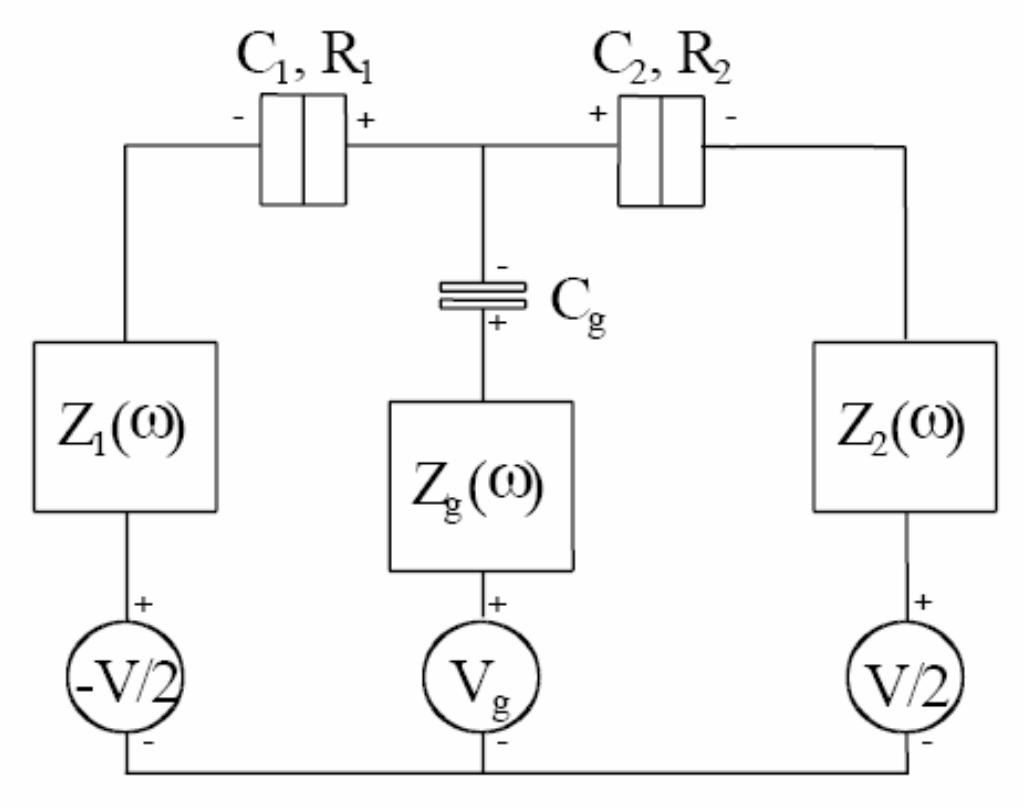

Figure 3.1. Single electron transistor with driving impedances. The tunneling resistances and capacitances of the double junction are R_1, C_1 and R_2, C_2, respectively. C_G is the gate capacitance. The Z's are the generator impedances of the driving (Z_1 and Z_G) and the output (Z_2).

$$E_{2r}(V,V_G,ne)=\frac{e}{C_\Sigma}\left[\left(C_1+\frac{C_G}{2}\right)V-C_GV_G-ne-\frac{e}{2}\right] \tag{3.3c}$$

$$E_{2l}(V,V_G,ne)=\frac{e}{C_\Sigma}\left[\left(C_1+\frac{C_G}{2}\right)V-C_GV_G-ne+\frac{e}{2}\right]\ , \tag{3.3d}$$

and the dimensionless energies η's are defined by

$$\eta_i(V,V_G,ne)=\beta E_i(V,V_G,ne)=\frac{E_i(V,V_G,ne)}{k_BT}\ \ (i=1r,1l,2r \text{ and } 2l)\ . \tag{3.4}$$

Here, C_Σ is the sum of the capacitances, $C_\Sigma=C_1+C_2+C_G$. Equation (3.2) shows that the tunneling rate depends only on the dimensionless energy, η_i, and the tunneling resistance at fixed temperature. At a given tunneling resistance and temperature Eq. (3.4) allows us to draw the different regimes of working, as shown in Figure 3.2 as a function of the source-drain voltage, V and the gate voltage, V_G. The maximal error rate $\Gamma^0_{SET}=3.17*10^{-8}Hz$, which corresponds to the limit of one-bit-error/transistor/year, is used as the condition of the error-free performance on Figure 3.2. The dotted lines represent the boundaries between the "on" and "off" states at zero temperature, while the solid lines represent the conditions of the maximal error rate in the "off" state. Each region represents different tunneling combination. The checked regions represent the zero current regions, defined by the maximal error rate, and their area is temperature dependent (see Eq. 3-4). These regions exist if the following conditions are satisfied simultaneously:

$$\eta_{jr}(V,V_G,ne)\le-\alpha^r_j(R_j,T)\ \text{ and }\ \eta_{jl}(V,V_G,ne)\ge\alpha^l_j(R_j,T)\ , \tag{3.5}$$

where we call the α's stability parameters. Equations (3-3), (3-4) and Relations (3-5) are used to generate Figure 3.2. It is important to note here that in order to have a reasonable estimation of the α's used in relation (3.5), we have proceeded in the following way. The actual values of the α's can be obtained from the following equations:

$$\frac{\Gamma^0_{SET}e^2R_j}{k_BT}=\frac{-\alpha^r_j(R_j,T)}{1-\exp\left[\alpha^r_j(R_j,T)\right]}\ , \tag{3.6a}$$

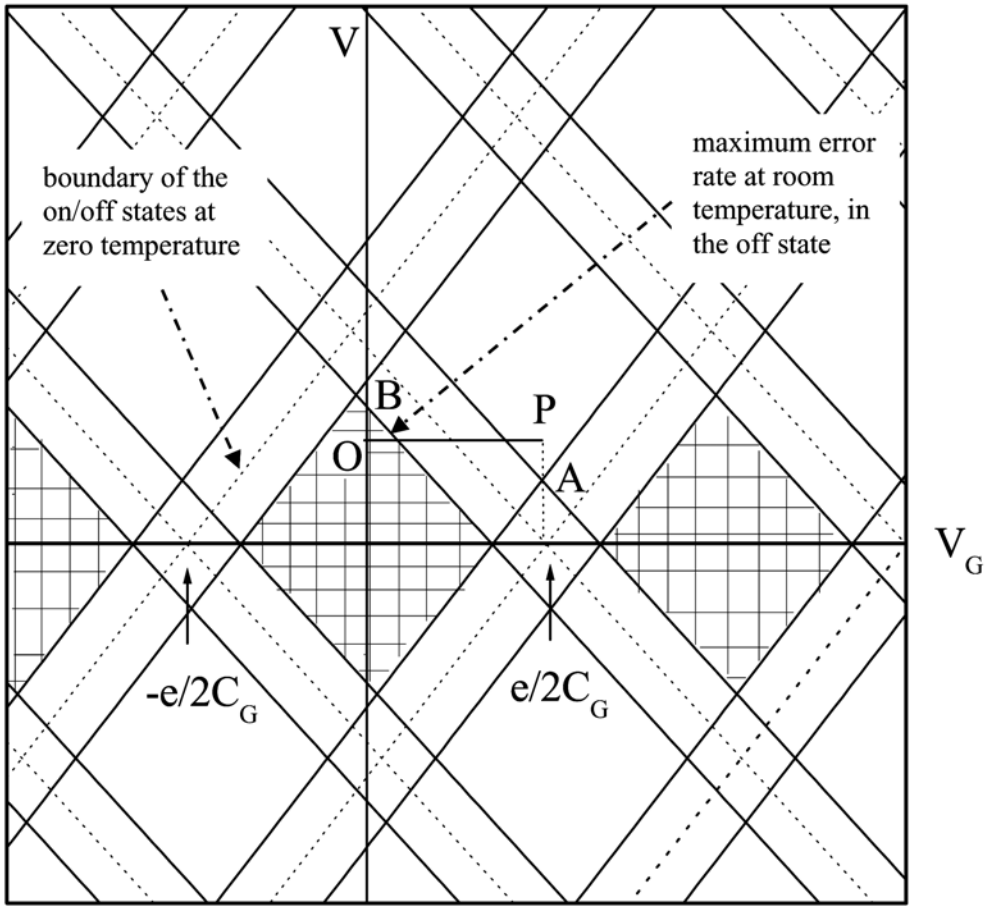

Figure 3.2. Working regimes of the single electron transistor with asymmetric junctions. With symmetric junctions, the figures would be symmetric on the axes. The dotted lines represent the boundaries between the "on" and "off" states at zero temperature, while the solid lines represent the conditions of the maximal error rate in the "off" state at room temperature. Point O and P represent "off" and "on" states.

or using the backward tunneling rate:

$$\frac{\Gamma^0_{SET} e^2 R_j}{k_B T} = \frac{\alpha^l_j\left(R_j, T\right)}{\exp\left[\alpha^l_j\left(R_j, T\right)\right] - 1} \quad \left(j = 1 \text{ and } 2\right) \ , \tag{3.6b}$$

where Eqs. (3-6a) and (3-6b) are relevant to the different tunneling direction and they give the same result for the α's. Figure 3.3 shows the dependence of the stability parameter, α, on temperature at the different tunneling resistance. It shows that although the α's are implicit functions of the tunneling resistance and temperature, they can be approximated by the following semi-empirical way:

$$\alpha\left(R_j, T\right) \ \cong \ \ln\alpha\left(R_j, T\right) - \ \ln\left(\frac{\vec{\Gamma}^Y e^2 R_j}{k_B T}\right) \cong \ \overline{\alpha} - n\ln\left(\frac{R_j}{10^6 T}\right) \quad , \tag{3.7}$$

where $\overline{\alpha} = 41.1$ and $n = 1.025$ for a single electron transistor[2]. After substituting the α obtained from Eq. (3.7) into Eq. (3.5), the error-free zero current condition is obtained from Eqs. (3.3) , (3.4), (3.5) and (3.7):

$$\frac{e^2}{2C_\Sigma} > \alpha\left(R_T, T\right) k_B T \ . \tag{3.8}$$

Eq. (3.8) expresses the condition of having the tunneling rate below the maximal error rate in the "off" state.

At practical operation the V and V_G has to satisfy two different kinds of requirements [16]. First, the drain voltage cannot be greater than $V^{\max}$ which corresponds to the maximal error rate in the "off" state. Second, in the "on" state, the gate should be driven by V_G^{opt} which provides the maximal possible current at given $V^{\max}$. Simple considerations based on Eqs. (3.3) lead to:

$$V^{\max} = \min\left\{ \frac{2}{2C_1 + C_G}\left(\frac{e}{2} - \frac{\alpha_1^r C_\Sigma k_B T}{e}\right), \ \frac{2}{2C_2 + C_G}\left(\frac{e}{2} - \frac{\alpha_1^r C_\Sigma k_B T}{e}\right)\right\} \tag{3.9a}$$

[2] The stability parameter also depends on the number *N* of the single electron transistors in a chip since the error rate is proportional to *N*. The maximal error rate for the chip with *N* single electron transistors is one bit-error/chip/year, i.e., $\Gamma^0_{chip} = \Gamma^0_{SET} / N$. For a chip with 10^9 single electron transistors, we get $\alpha_{10^9} \cong 62.25 - 1.025\ln\left(10^6 / R_T T\right)$.

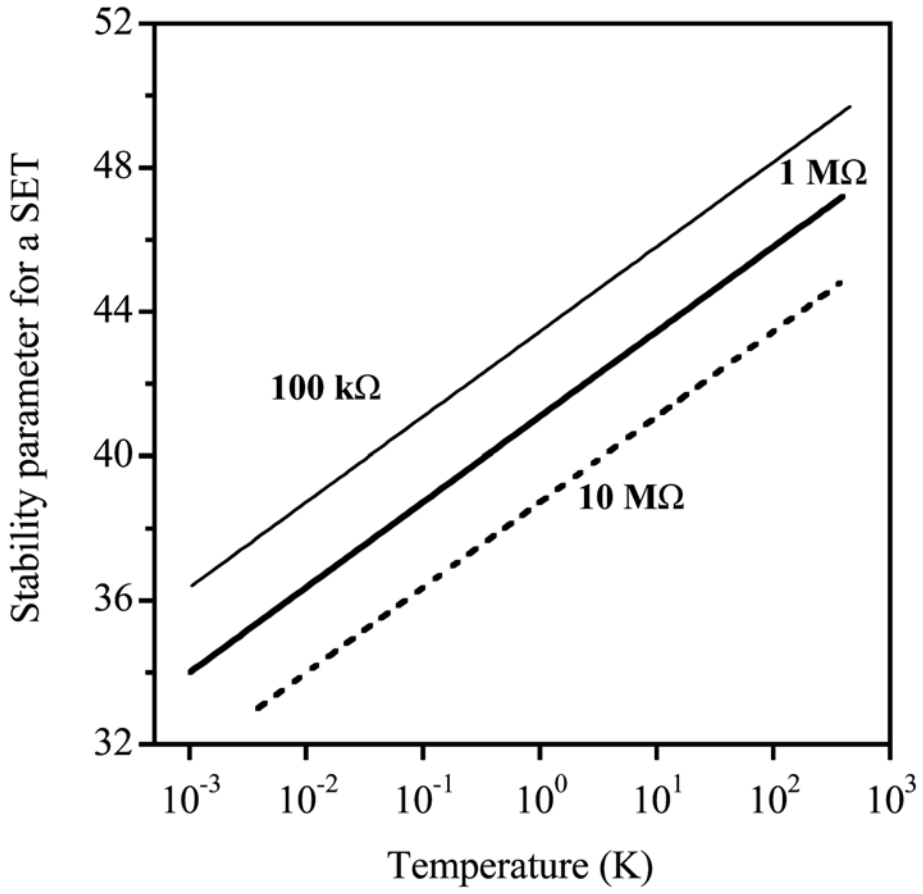

Figure 3.3. Stability parameter as a function of temperature. It is evaluated by Equation (3.6).

and

$$V_G^{opt} = \frac{e}{2C_G} + \frac{\left[\left(2C_1 + C_G\right)\alpha_1 - \left(2C_2 + C_G\right)\alpha_2\right] k_B T}{2eC_G} \tag{3.9b}$$

where $\alpha_j = \alpha\left(R_j, T\right)$ and min(a, b) represents the minimum of a and b. If the two junctions are symmetric, i.e., $C_1 = C_2$, $R_1 = R_2 = R$, then Eqs. (3.9) will be simplified so that the operation voltages in the "on" state become $V^{\max} = e/2C_\Sigma$ and $V_G^{opt} = e/2C_G$. In this case, we have the maximal rate of electron flow through the device (refer to Eq. (A.14)):

$$\vec{\Gamma}_t = \frac{1}{8C_\Sigma R\left[1 - \exp\left(-\beta e^2/4C_\Sigma\right)\right]} \cong \frac{1}{8C_\Sigma R} \quad . \tag{3.10}$$

Eq. (3.10) is based on unidirectional tunneling because tunneling in the reverse direction would be negligible at the maximal tunneling rate conditions.

When the transistor runs at the maximal clock frequency, the dissipation power of a single electron transistor with symmetric junctions is

$$P_1 = e \cdot \vec{\Gamma}_t \cdot V_G^{opt} = \frac{e^2}{16C_G C_\Sigma R}. \tag{3.11}$$

It is important to note that this is the ultimate lower limit of dissipation because Eq. (3.11) takes into the account only the energy needed to control the device. The actual power dissipation of the device is not included in this picture because it can be dependent on several other conditions.

3.2. Size Dependence

In general, the semiconductor single electron transistor is built in lateral structure which has 2-dimensional electron gas. In the lateral structure, the quantum dot of the single electron transistor is supposed to be a flat circular disk. Therefore, using the size dependence of the geometric capacitance, $C_\Sigma = 8\varepsilon R_{QD}$ [17], we obtain the following relations for the size dependence of the error-free performance condition:

$$R_{QD} \le \frac{e^2}{16\varepsilon\alpha\left(R,T\right) k_B T} \quad , \quad \vec{\Gamma} \cong \frac{1}{64\varepsilon R_{QD} R} \quad , \quad P_1 = \frac{e^2}{128\varepsilon C_G R_{QD} R} \quad . \tag{3.12}$$

where ε is the permittivity of insulator and R_{QD} is the radius of a flat circular disk. Eq. (3.12) holds for single electron transistor with symmetric junctions.

Today, the number of MOS transistors in the Pentium 4 microprocessor is about 100 millions/cm^2 and the characteristic size of lithography is around 100nm. Comparing this transistor density with the case of densely packed transistors, we can see that the transistor packing density $\theta = 0.01$, where θ is the ratio of the actual number transistors to the number of devices of the characteristic size at fully dense packing. From Eq. (3.12), the power dissipation of a chip with N single electron transistors can be given as

$$P_N = N * P_1 = N \frac{e^2}{128 \varepsilon C_G R_{QD} R} \approx \theta \frac{10^{-4}}{R_{QD}^2} \frac{e^2}{128 \varepsilon C_G R_{QD} R} = \frac{10^{-4} e^2 \theta}{128 \varepsilon C_G R_{QD}^3 R} \quad . \qquad (3.13)$$

It should be noted that this is the lower limit of power dissipation of the chip because the dissipation of other elements are neglected.

Figure 3.4 shows the lower limit of power dissipation (when running at the maximal clock frequency); the maximal clock frequency of the one single electron transistor; and the power dissipation of 10^9 single electron transistors. Here, $\varepsilon = 3.9 \varepsilon_0$ for SiO_2 , $R = 1\text{M}\Omega$ and $C_G / C_\Sigma = 0.1$ are assumed. It is apparent from Eqs. (3.12) and (3.13) and from the slope of curves in Figure 3.4 that $f_{MAX} \propto R_{QD}^{-1}$, $P_1 \propto R_{QD}^{-2}$, and $P_N \propto R_{QD}^{-4}$. It is important to point out that the power dissipation limits of chips, which is in 2003 about 100 W, sets another upper limit for the clock frequency. When the maximal power dissipation of the chip is limited at 100 W, the radius of the quantum dot and the maximal clock frequency are about 6 nm and 30 GHz, respectively. It implies that microprocessors with $R_{QD} \le 6\text{nm}$ cannot operate at the maximal clock frequency f_{MAX}. In fact, the maximal clock frequency is less than Eq. (3.11) due to shot noise [4].

Finally, we study the maximal quantum dot size versus temperature. The results are compared by a simple prediction based on the level-crossing analysis of thermal noise at given capacitance and bandwidth. The rms thermal noise voltage $V_n = \sqrt{k_B T / C_G}$ on the capacitor and the practical noise margin $V_G^{opt} \ge 12 V_n$,which Kish found, yields the following relation:

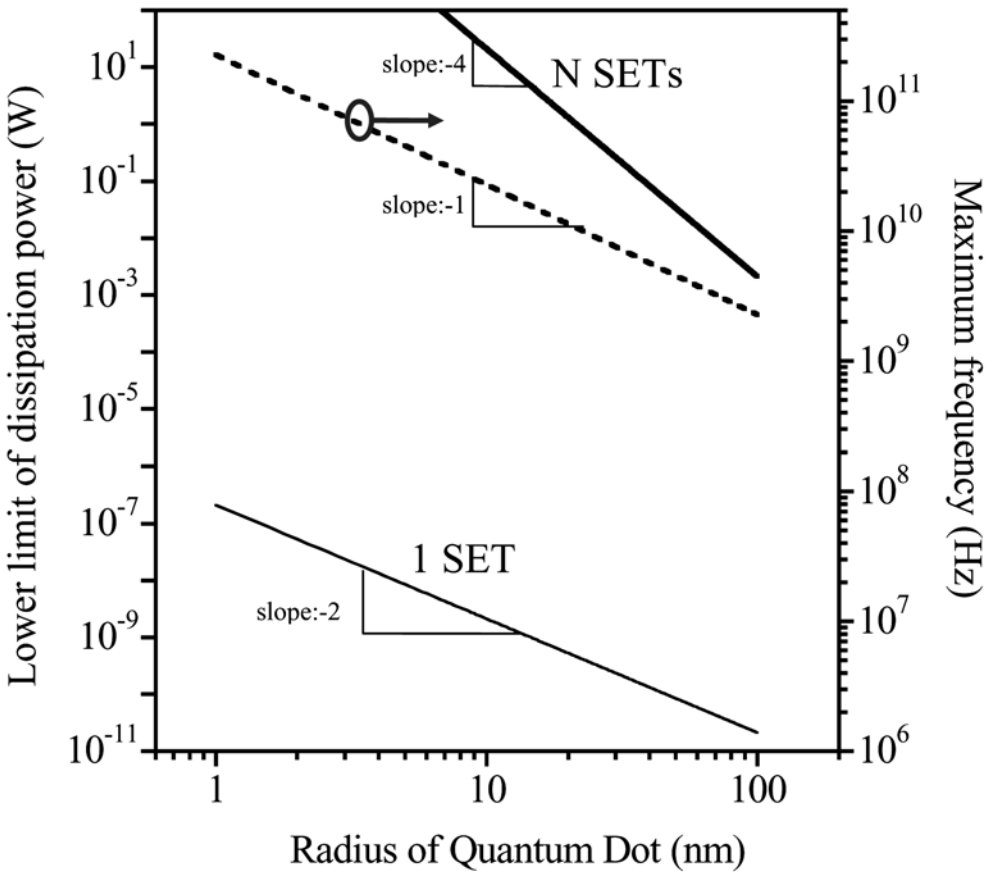

Figure 3.4. Lower limit of power dissipation in single electron logic processors. Power dissipation of a single electron transistor and a chip with N single electron transistors, and the maximal clock frequency are a function of the radius of the quantum dot. The same packing density θ=0.01 is supposed as in today's microprocessor chips.

$$C_G \le \frac{1}{576}\frac{e^2}{k_B T} \quad . \tag{3.14}$$

In Figure 3.5, the thin solid line represents the case where the charging energy is equal to thermal energy, i.e. the device can be used only as a DC switch which is not suitable for error-free data manipulation. Surprisingly, the simple thermal noise estimation works very well at large quantum dot limit. However, as the size of the quantum dot decreases, the size quantization effect becomes dominant[3]. That case has a different slope[4] because $T \propto R_{QD}^{-1/2}$. So, the size quantization effect is a beneficial effect which helps to work at higher temperatures or bigger sizes. The analysis of Figure 3.5 suggests that a processor including 10^9 single electron transistors with smaller than 1 nm quantum dot size can work at room temperature.

[3] For Si/SiO_2, the radius of the quantum dot is 2.8 nm at which the ratio of energy level spacing in quantum dot to electrostatic charging energy, $E_{QD}/E_C = 4\pi\hbar^2 C_\Sigma / m_e e^2 A_{QD}$ is unit. Here m_e is the effective mass of the electron and A_{QD} is the area of the quantum dot.

[4] The energy level spacing from the size-quantization effect is proportional to $1/R_L^2$ where R_L is the characteristic length of the quantum dot. Since the thermal energy is much less than the spacing between energy levels, the maximum characteristic length of the quantum dot satisfies $\log(R_L)_{MAX} \propto (-1/2)\log T$.

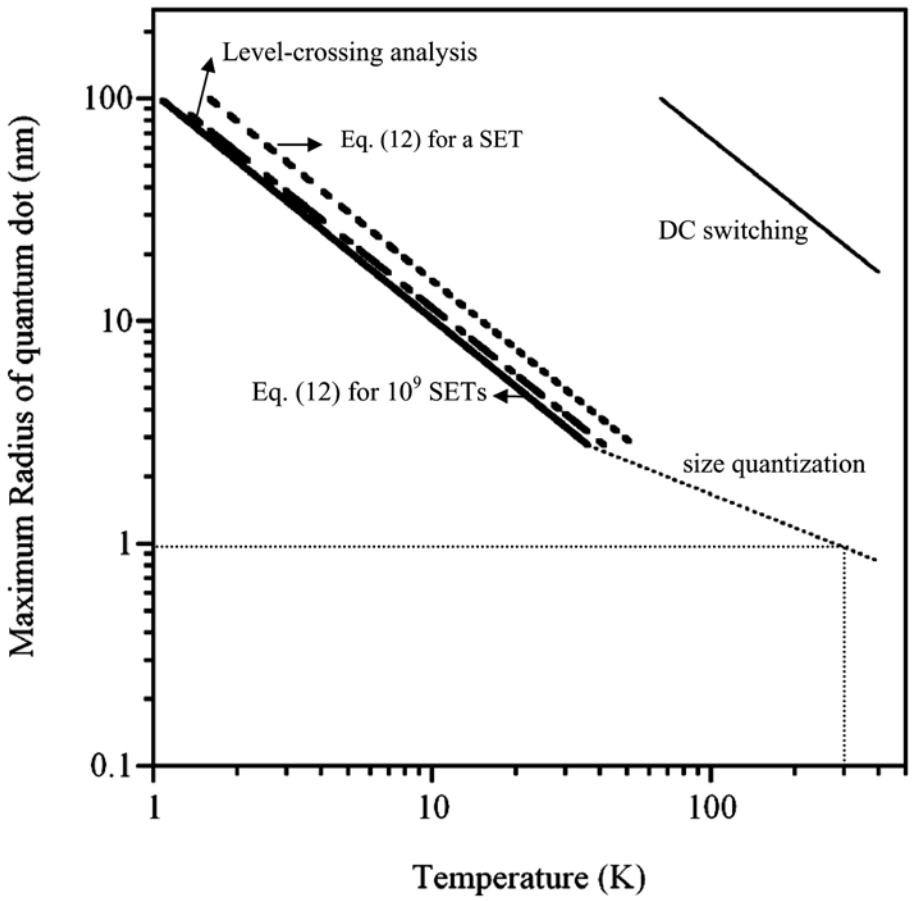

Figure 3.5. Maximum radius of the quantum dot for operation at given temperature. The thin solid line represents the requirement of efficient DC switching (on/off) of the device. The other lines give the maximal size for the error-free performance. The dashed line is for a single electron transistor. The rest of the lines are for a chip with 10^9 single electron transistors. The thick solid line is given by Eq. (3.12), the dashed-dotted line is given by the thermal noise level-crossing analysis, and the dotted line estimates the case where the size-quantization effect dominates; it is extrapolated below 2.8 nm.

4. SUMMARY

We have studied current-controlled logic and single electron logic processors with respect of error rate. The study showed some fundamental limits of information processing in current controlled logic with shot noise. With 100 million transistors, such as Pentium 4, and with the assumption of a maximal supply current of 100 A, the maximal clock frequency would be 10 GHz in a current-controlled logic processor.

In a single electron logic processor, the aspects of thermal-induced noise have been studied versus the radius of quantum dot. The analysis showed that a single electron logic processor with silicon quantum dots of less than 1nm radius can work without error at room temperature, and that it has to be in the size quantization mode.

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APPENDIX

In appendix, we will summarize Ingold and Nazarov's work [14] about single electron tunneling rate of an ultrasmall junction, and Ingold, Wyrowski and Grabert's work [15] about the tunneling rate in a single electron transistor.

Figure A.1 shows an ultrasmall tunneling junction connected to an ideal voltage source V and an external impedance $Z(\omega)$. Since the tunneling is a quantum effect, the Hamiltonian of the circuit has to be treated in quantum mechanical way. The total Hamiltonian of the circuit including the junction, shown in Figure A.1, is separated into three parts:

$$H = H_{ld} + H_{env} + H_T \tag{A.1}$$

where H_{ld} is the Hamiltonian of dressed electrons in leads, H_{env} the Hamiltonian of the electromagnetic environment related to the external impedance and H_T the Hamiltonian from the tunneling. The Hamiltonian of the dressed electrons in leads is

$$H_{ld} = \sum_{k\sigma} (\varepsilon_k + eV) c_{k\sigma}^{\dagger} c_{k\sigma} + \sum_{q\sigma} \varepsilon_g c_{g\sigma}^{\dagger} c_{g\sigma} \tag{A.2}$$

where the first and second summation is Hamiltonian of left and right electrodes, respectively, and ε_k and ε_g are the energies of the dressed electrons with wave vector k and g. Here $c_{k\sigma}$ and $c_{k\sigma}^{\dagger}$ represents the annihilation and creation operators of the electron with wave vector k and spin σ, respectively. The Hamiltonian of the tunneling is

$$H_T = \sum_{k\,g\,\sigma} T_{kg}\, c_{g\sigma}^{\dagger}\, c_{k\sigma}\, e^{-i\tilde{\varphi}} + \text{Hermitian Conjugate} \tag{A.3}$$

where T_{kg} is the matrix element that corresponds to the tunneling from an electron with vector k at the left lead to an electron with vector g at the right lead, and $\tilde{\varphi}$ the phase[5] fluctuation from the phase determined by the voltage source at the junction. The hermitian

[5] The phase is defined as $\varphi(t) = \frac{e}{\hbar}\int_{-\infty}^{t} dt' U(t')$ where $U(t) = Q/C$ is the voltage across the junction.

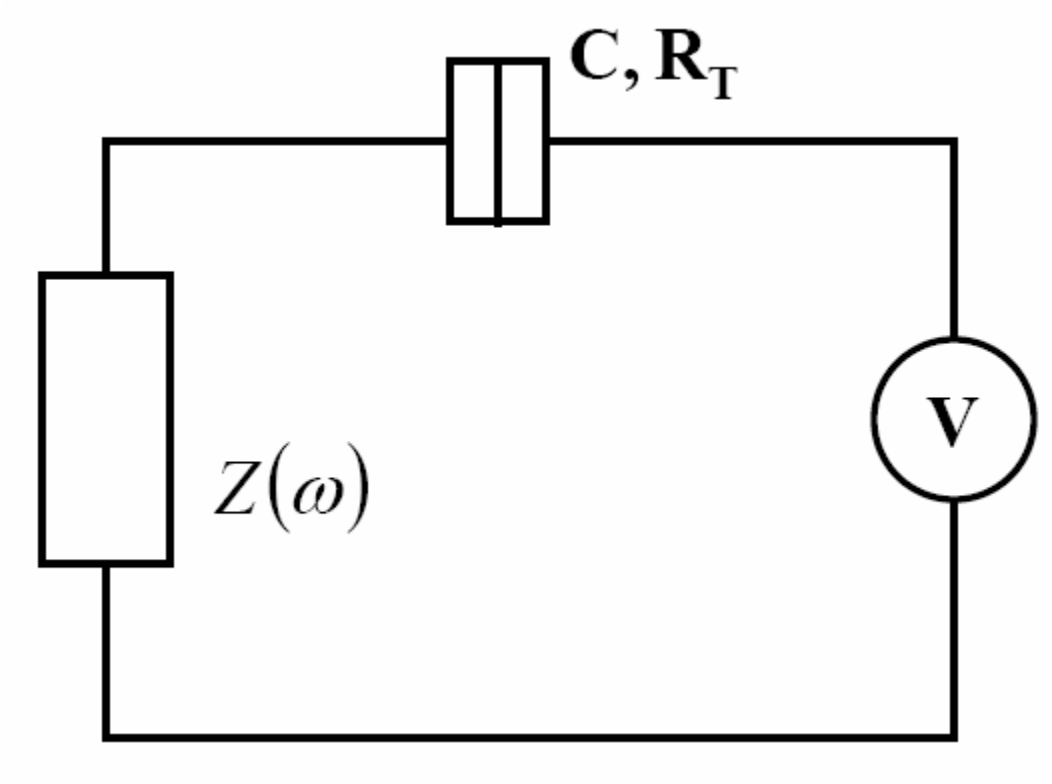

Figure A.1. Single electron junction with an ideal voltage source and an external impedance.

conjugate term represents the hermitian conjugate of the first, which describes the reverse tunneling. And, provided that the electromagnetic environment consists of coupled N_e LC harmonic oscillators, the Hamiltonian of the electromagnetic environmental is

$$H_{env} = \frac{\tilde{Q}^2}{2C} + \sum_{n=1}^{N_e}\left[\frac{q_n^2}{2C_n} + \left(\frac{\hbar}{e}\right)^2 \frac{1}{2L_n}\left(\tilde{\varphi} - \varphi_n\right)^2\right] \tag{A.4}$$

where $\tilde{Q}$ is the charge fluctuation from the mean charge, CV, on the ultrasmall junction, q_n and L_n are, respectively, the capacitance and the inductance of the n[th] LC harmonic oscillator. Using Fermi's golden rule and considering that the eigenstates of this system consist of the energy states, $|E\rangle$, and the reservoir states, $|R\rangle$, give the total rate of electron tunneling from left to right

$$\vec{\Gamma} = \frac{2\pi}{\hbar}\int dE\, dE' \sum_{kq\sigma RR'} \left|\langle E'|T_{kq}\, c_{q\sigma}^{\dagger}\, c_{k\sigma}\,|E\rangle\right|^2 \left|\langle R'|e^{-i\tilde{\varphi}}\,|R\rangle\right|^2 P_\beta(E) P_\beta(R)\,\delta\left(E + eV + E_R - E' - E_{R'}\right)$$

where the prime stands for the final state, $P_\beta(E)$ is the probability of finding the state with energy E at temperature T, and E_R the energy of the state $|R\rangle$. Since the only tunneling-possible case is where the state with vector k at the left is occupied, but the state with g at the right is empty, $P_\beta(E) = f(\varepsilon_k)\left[1 - f(\varepsilon_g)\right]$ where $f(\varepsilon)$ is the Fermi-Dirac function and $\left|\langle E'|T_{kg}\, c_{g\sigma}^{\dagger}\, c_{k\sigma}\,|E\rangle\right|^2 = |T_{kg}|^2$. Introducing tunneling resistance $R_T = \hbar \Big/ \left(2\pi e^2 \sum_{kg\sigma} |T_{kg}|^2\right)$, the total rate is rewritten as

$$\vec{\Gamma} = \frac{1}{e^2 R_T}\int_{-\infty}^{+\infty} dE\, dE'\, f(E)\left[1 - f(E')\right] \sum_{RR'} \left|\langle R'|e^{-i\tilde{\varphi}}\,|R\rangle\right|^2 P_\beta(R)\,\delta\left(E + eV + E_R - E' - E_{R'}\right)$$

Here, it is assumed that R_T is independent of the energies, E and E'. Using the definition of the delta function, i.e., $\delta(E) = \int_{-\infty}^{+\infty} dt \exp(iEt/\hbar) \Big/ 2\pi\hbar$, introducing the time dependent phase operator in the Heisenberg picture and then using $\int_{-\infty}^{+\infty} dE\, f(E)\left[1 - f(E + x)\right] = x \Big/ \left(1 - e^{-x/k_B T}\right)$ gives the total rate of electron from left to right as

$$\vec{\Gamma} = \frac{1}{e^2 R_T}\int_{-\infty}^{+\infty} dE\ \frac{E}{1-\exp\left(-E/k_B T\right)} P\left(eV-E\right) \tag{A.5}$$

where $P\left(eV-E\right)=\sum_{R,R'} P_\beta\left(R\right)\left\langle R\left|e^{-i\tilde{\varphi}(t)}\right|R'\right\rangle\left\langle R'\left|e^{-i\tilde{\varphi}(0)}\right|R\right\rangle$. $P\left(eV-E\right)$ is the probability to emit the energy difference between two leads, $E-E'$, to the external circuit, and it depends on the electromagnetic environment. The total tunneling rate of electron from left to right is evaluated from Equation (A.5) if the property of the environment, i.e., $P\left(eV-E\right)$ is known. The total backward tunneling rate of electron from right to left can be calculated in the above way. However, since the backward tunneling rate of electron at the positive biased voltage is the same as the forward tunneling rate at the negative biased voltage, the total backward tunneling rate is

$$\overleftarrow{\Gamma}\left(V\right)=\vec{\Gamma}\left(-V\right) \tag{A.6}$$

If the impedance of the electromagnetic environment is very low, the environment effect may be negligible. Therefore, $P\left(eV-E\right)=\delta\left(eV-E\right)$ and the total tunneling rate of electron from left to right is at a given temperature T

$$\vec{\Gamma}\left(V\right)=\frac{1}{e^2 R_T}\frac{eV}{1-\exp\left(-eV/k_B T\right)} \tag{A.7}$$

Single electron transistor is shown in Figure 3.1. As we said in the above, we will summarize the tunneling rate through double junction in the single electron transistor. The transistor has a Coulomb island (or quantum dot) between the junctions. The tunneling rate at each junction is dependent on the excess charge at the island. Here, we are interested in a low impedance single electron transistor since low impedance leads to the high clock frequency of the microprocessor. Therefore, all of external impedances in Figure 3.1 are neglected in the evaluation of the tunneling rate. The effective voltage across the first junction in the single electron transistor shown in Figure 3.1 is

$$\overline{V_1}=\left[\left(C_2+C_g/2\right)V+C_g V_g\right]/\left(C_1+C_2+C_g\right) \tag{A.8}$$

$e\overline{V_1}$ is the work that is necessary to reestablish charge equilibrium after single electron tunneling. The effective voltage across the second junction is

$$\overline{V_2}=-\left[\left(C_1+C_g/2\right)V-C_g V_g\right]/\left(C_1+C_2+C_g\right) \tag{A.9}$$

where the negative sign is due to the polarity of the second junction in Figure 3.1. The effective energy that is required by the tunneling and the equilibrium recovery is

$$E_1(V,V_g,q)=\frac{q^2}{2C_\Sigma}-\frac{(q-e)^2}{2C_\Sigma}+e\overline{V_1} \tag{A.10}$$

where q is the excess charge at the island, ne, and C_Σ is the sum of all capacitances. Here, the first two terms on the right hand side are due to the electrostatic charging energy, and the last is due to the work done by the voltage sources in restoring equilibrium. Since the '$-e$'excess charge is added to the island in the calculation of the energy E_1, the single electron tunnels from the left of the first junction to the right. Replacing eV in equation (A.7) by equation (A.10), E_1, gives the (forwarding) tunneling rate of the electron from the left of the first junction to the right

$$\vec{\Gamma}_1(V,V_g,q)=\frac{1}{e^2R_1}\frac{E_1(V,V_g,q)}{1-\exp\left(-E_1(V,V_g,q)/k_BT\right)} \tag{A.11}$$

Considering the discussion above the equation (A.6), the backward tunneling rate at the first junction is

$$\overleftarrow{\Gamma}_1(V,V_g,q)=\vec{\Gamma}_1(-V,-V_g,-q) \tag{A.12}$$

For the forward tunneling at the second junction, the effective energy E_2 is

$$E_2(V,V_g,q)=\frac{q^2}{2C_\Sigma}-\frac{(q+e)^2}{2C_\Sigma}-e\overline{V_2} \tag{A.13}$$

, and the forward tunneling rate is obtained by changing the index 1 to 2 in equation (A.11). As shown in equations (A.7) and (A.11), the tunneling rate through each junction depends on the system temperature.

Finally, the effective rate of electron to pass through the double junction is

$$\frac{1}{\Gamma(V)}=\frac{1}{\vec{\Gamma}_1(V,0)}+\frac{1}{\vec{\Gamma}_2(V,-e)} \tag{A.14}$$

when the source-drain voltage is so small that the excess charge at the quantum dot is only zero or $-e$.

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